Printed Microprocessors

Nathaniel Bleier
UIUC

Muhammad Husnain Mubarik
UIUC

Farhan Rasheed
KIT

Jasmin Aghassi-Hagmann
KIT

Mehdi B Tahoori
KIT

Rakesh Kumar
UIUC

Abstract

Printed electronics holds the promise of meeting the cost and conformality needs of emerging disposable and ultra-low cost margin applications. Recent printed circuits technologies also have low supply voltage and can, therefore, be battery-powered. In this paper, we explore the design space of microprocessors implemented in such printing technologies - these printed microprocessors will be needed for battery-powered applications with requirements of low cost, conformality, and programmability. To enable this design space exploration, we first present the standard cell libraries for EGFET and CNT-TFT printed technologies - to the best of our knowledge, these are the first synthesis and physical design ready standard cell libraries for any low voltage printing technology. We then present an area, power, and delay characterization of several off-the-shelf low gate count microprocessors (Z80, light8080, ZPU, and openMSP430) in EGFET and CNT-TFT technologies. Our characterization shows that several printing applications can be feasibly targeted by battery-powered printed microprocessors. However, our results also show the need to significantly reduce area and power of such printed microprocessors. We perform a design space exploration of printed microprocessor architectures over multiple parameters - datawidths, pipeline depth, etc. We show that the best cores outperform pre-existing cores by at least one order of magnitude in terms of power and area. Finally, we show that printing-specific architectural and low-level optimizations further improve area and power characteristics of low voltage battery-compatible printed microprocessors. Program-specific ISA, for example, improves power, and area by up to 4.18x and 1.93x respectively. Crosspoint-based instruction ROM outperforms a RAM-based design by 5.77x, 16.8x, and 2.42x respectively in terms of power, area, and delay.

1. Introduction

Computing devices and systems are pervasive today and have an ever increasing footprint. Every major evolutionary step in computing - from high performance computing, to personal computing, to mobile computing, and to internet-of-things (IoTs) - has led to a quantum increase in the number of computing devices and systems. Tens of billions of IoT devices (wearables [38], implantables [100], sensors [108], RFIDs [10], etc.), for example, are expected to be shipped in next five years [106].

Surprising as it may sound, a vast set of domains - especially disposables with ultra-low cost margins and conformality requirements - still have not seen much proliferation of computing. Example domains include 1) packaging [91] and in-situ monitoring [32] for fast moving consumer goods (FMCG), 2) patches for monitoring health [34, 77, 41, 43], activity [88], posture [68], and sleep [117], 3) low-end healthcare products such as smart bandages [78], and 4) disposable sensors for food [28], forensics [33], pharmaceuticals [69], agriculture [55], and environment [66].

The primary reasons why such domains have not seen significant penetration of computing are cost and conformality. Consider cost. While silicon costs are already quite low (one can buy a microcontroller today for less than a dollar [2]; one can buy Java cards for low tens of cents [1]), they are still considerably higher than the cost needs for some of these domains. For example, for item-level tagging applications (e.g., in packaging), electronics needs to be as cheap as a barcode (sub-cents [95]). An empty beer bottle [7], an empty soda can [8], or a single bandage [9] cost only a few cents. The corresponding electronics needed to make them "smart", again, need to cost less than a cent. High manufacturing, packaging, testing, and assembly costs of silicon have prevented sub-cent costs. Similar argument holds true for conformality as well - many applications [99, 20, 118, 125] have stretchability, porosity, and flexibility requirements that cannot be met by silicon.

There has been considerable interest in printed electronics technology, as a way to target disposables and ultra-low cost margin domains, especially with conformality needs. Printing technologies, especially those based on maskless and additive processes, can dramatically reduce the cost of manufacturing [103] as well as production timeline. Several printing technologies (e.g., inkjet printing) can also be portable ("fab-in-a-box") which reduces cost even further since a circuit can be manufactured on-demand at the point-of-use. Printed electronics can also be flexible [17], stretchable [114], porous [112], and non-toxic - these attribute make printed electronics even better fit for several disposable ultra-low-cost applications such as smart packaging and on-body patches.

While some of the above benefits of printing have been known for quite some time, some relatively recent developments have made printed electronics particularly attractive. Past research on printed devices largely focused on displays and OLEDs [62] as target applications. Unsurprisingly, corresponding transistors had high supply voltage (e.g., $> 5\,V$) and poor mobility values, making them a poor fit for battery-powered applications. Technologies such as carbon nanotube based thin-film transistor (CNT-TFT)[67] have emerged re-

cently that have low supply voltage and relatively high electron mobility (Table 1). This has opened a gateway for printed battery-powered applications. Most disposable ultra-low-cost applications discussed above fall in this category. Furthermore, while prior work on printed electronics was largely focused on organic transistors, several transparent oxide-based inorganic printed technologies [113, 120] have emerged recently. Transparent oxides have much higher (one order of magnitude) mobilities than organic semiconducting polymers [36]. Also, compared to the conventional inorganic channel based TFTs that have high operating voltages ($> 30\,V$) and very low mobility values ($< 1\,cm^2/Vs$) [89], the new inorganic technologies (e.g., electrolyte-gated FET - EGFET) have much better supply voltage and mobility characteristics (Table 1), making them much better fit for battery-powered applications.

Table 1: Comparison between different printed/flexible electronics technologies in terms of operating voltage and mobility (OTFT = Organic Thin-Film Transistor, IOTFT = Inorganic Thin-Film Transistor) for inkjet and shadow mask printing

Process Technology	Processing Route	Operating Voltage [V]	Mobility [cm^2/Vs]
EGFET [12]	Inkjet	<1	126 [37]
IOTFT [89]	Solution/inkjet	40	1
OTFT [85]	Inkjet	30	$2e^{-4}$
OTFT [18]	Inkjet	50	0.02
OTFT [57]	Gravure-inkjet	15	1
Carbon Nanotube [97]	Solution/ shadow mask	1-2	25 [67]
OTFT [16]	Shadow mask	5-10	0.16
SAM OTFT [64]	Shadow mask	2	0.5
OTFT [84]	Shadow mask	20-40	11

In this work, we focus on printed microprocessors. There are several reasons to consider printing microprocessors. Although printing reduces the manufacturing costs, overall cost may still be dominated by design, test, and verification costs. A printed microprocessor helps amortize these costs over greater volume compared to any printed application-specific design. Second, programmability may still be important, even in disposable and ultra-low cost margin domains, -e.g., consider the ability to change prices of FMCG items on shelves, the ability to change monitoring frequency and monitored characteristics based on acquired data, the ability to tune learning algorithms for a specific person, etc. Finally, in a sensor-based application, if the sensor is to be printed (perhaps due to conformality, customizability, or cost benefits), it may often make sense to print a microprocessor alongside the printed sensor to enable near-sensor computing on the printed sensor data (e.g., for latency, energy, privacy, or security reasons), while reducing the integration costs of the final system (i.e., benefit of using a single process for all components of the system).

No prior work has explored the design space of printed microprocessors in low voltage printed technologies. It is not surprising since such exploration requires Process Design Kits (PDKs) that have started becoming available only recently [124, 98, 122, 13, 16]. In fact, to the best of our knowledge, there does not exist any synthesis and physical design ready standard cell library for low voltage printed electronics. Such a library is a pre-requisite for an architectural exploration.

Our study produces several architectural insights. First, since DFFs are considerably more expensive than combinational cells for EGFET/CNT-TFT (Table 2), the best printed microprocessor cores are single-stage pipelines (Figure 7). Second, large DFF overheads encourage printed processor designs without a register file. Third, to support cores without registers, memory-memory ISA becomes an attractive ISA choice for printed microprocessors (Figure 6). Alternatives such as stack-based ISA have high overhead due to the high overhead of RAM-based stack implementation (RAM is considerably more expensive than ROM in EGFET/CNT-TFT - Table 6). Similarly, CISC ISAs have high gate and DFF count and are difficult to implement in single cycle. Fourth, a Harvard organization fits better than a Von-Neuman organization since it allows instructions to be placed in a dense crosspoint-based ROM (Section 6). Fifth, on-demand fabrication enabled by technologies such as inkjet printing enable program-specific processors (Section 7).

This paper makes the following contributions:

- We present (Section 3) standard cell libraries for EGFET and CNT-TFT printed technologies. To the best of our knowledge, these are the first synthesis and physical design ready standard cell libraries for any low voltage printing technology. These libraries, made public for broader use[1], are critical for design space exploration of battery-powered printed microprocessors
- We present (Section 4) an area, power, and delay characterization of low gate count microprocessors (Z80, light8080, ZPU, openMSP430) in EGFET and CNT-TFT technologies. Our characterization shows that several printing applications can be feasibly targeted by battery-powered printed microprocessors. Our results also show the need to significantly reduce area and power of such printed microprocessors.
- We perform (Section 5) a design space exploration of printed microprocessor architectures over multiple parameters-datawidths, pipeline depth, etc. We show that the best cores outperform pre-existing cores by at least an order of magnitude in terms of area and power. Our exploration also discovers interesting tradeoffs that can guide optimization of battery-powered printed processors.
- We show (Section 8) that printing-specific architectural and low-level optimizations can be used to further improve power and performance characteristics of battery-powered printed microprocessors. Program-specific ISA

[1] https://www.github.com/PrintedComputing

(Section 7), for example, improves power and area by up to 4.18x and 1.93x respectively, with minor variation in f_{max}. Crosspoint-based instruction ROM (Section 6) outperforms a RAM-based design by 5.77x, 16.8x, 2.42x respectively in terms of power, area, and delay.

2. Background and Related Work

Printed electronics is an all-encompassing term used to denote a set of emerging printing technologies which enable flexible, on demand, and low-cost fabrication process for electronic devices on various substrates [21]. Printing technologies are broadly divided into two categories (Figure 1). Some printing technologies are based on purely additive manufacturing process, while others employ subtractive process as well [15]. In the subtractive process, a series of additive (deposition) and subtractive (etching) steps are involved, similar to the silicon based processing. The subtractive process is relatively expensive compared to the additive process as it involves highly specialized processing, expensive equipment, and infrastructure [14]. On the other hand, only deposition steps are involved in the additive manufacturing process. Transistors, passive components, and interconnects are realized by depositing material layer-by-layer. Fully-additive printed electronics (e.g., inkjet-printed EGFET), in general, are slower compared to the subtractive-based printed technologies (e.g., solution/shadow mask-printed CNT-TFT).

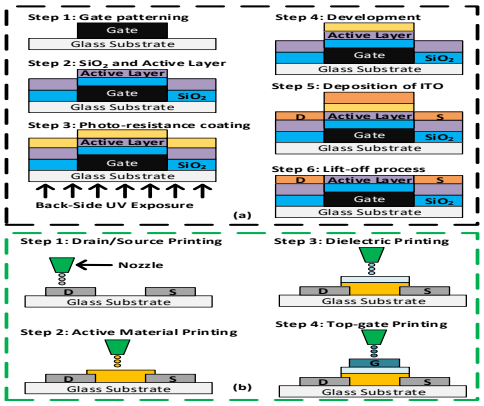


Figure 1: (a) Subtractive based printing process (b) Fully-additive inkjet printed process

Printed electronics do not compete with silicon-based electronics in terms of integration density, area and performance. Typical frequencies achieved by printed circuits are in the range of few Hz to a few kHz [44, 11]. Similarly, the feature size tends to be several microns [72, 67, 115].

The input voltage of printed electronics can range from over 10 V [73, 65] to less than 1 V [72, 115] for ion gel or electrolyte-gated technologies (Table 1), making these recent technologies suitable for battery-powered applications.

The cost of fabricating printed circuits can be considerably lower than the cost of silicon-based circuits. As an example, a standard Dimatix Materials Printer DMP-2831 (Figure 3) used to print EGFET-based [72] circuits costs less than 50000 dollars. In contrast, hundreds of millions of dollars are needed for even the older silicon foundries [46]. The promise of printing is that these low fabrication costs can be used to target disposable and ultra-low cost margin application domains. Once stretchability, flexibility, porosity, and non-toxicity benefits of printed circuits are considered, printed electronics become compelling for several applications.

Prior work on printing active electronics has largely focused on fabricating simple circuits (e.g., basic digital blocks [115, 65], ring-oscillators [44, 11, 59, 127], amplifiers [14, 63] Digital-to-Analog and Analog-to-Digital converters [14, 116], shift registers [67] and memories [123, 51]. The closest related work on printed or conformal processors are [80, 79, 16, 49]. The processor reported in the [80] is an 8-bit microprocessor fabricated on a flexible substrate. It operates at 10 V with a back-gate voltage of 50 V which is prohibitively high for the battery-powered applications that we are interested in. The other processor [79] is also an 8-bit microprocessor with a programmable write-once, read-many (WORM) memory. It is 52x faster than [80]. However, the typical supply voltage is the same (12 V) with a minimum of 6.5 V that makes it inadequate for battery-powered applications. Also, both [80] and [79] use relatively expensive fabrication equipment compared to the inkjet printing process, making them less attractive for low-cost applications. The work in [16] is focused on architectural optimization of an organic thin-film transistor (OTFT)-based biodegradable processor. However, the technology is based on shadow mask process with a typical supply voltage range between 5 V to 10 V. Such high voltages may not be compatible with the needs of battery-powered applications. Also, shadow mask-based printing is subtractive, making it considerably more expensive than additive inkjet-based EGFET-based designs that we primarily focus on. Hills *et al* [49] present a 16-bit CNTTFT-based microprocessor based on RISC-V instruction set. Again, the printing technology involves subtractive processing steps. Another related project is PlasticARM [105], a 10,000 gate NMOS-based SOC (32-bit CPU, memory and peripherals) research prototype on plastic substrate. However, not many other details are public.

There is some related work on PDKs for printing technologies [124, 98, 122, 13, 16]. However, most of them do not include a synthesis and physical design standard cell library, which is crucial for digital circuit design and evaluation.

3. Enabling Standard Cell-based Design of Low Voltage Printed Microprocessors

In this section, we provide an overview of two low-voltage printing technologies - EGFET [12] and CNT-TFT [67] - with considerably different tradeoffs. While EGFET printing is fully additive (inkjet-based), and low cost, CNT-TFT is subtractive, higher cost, and considerably more performant. We

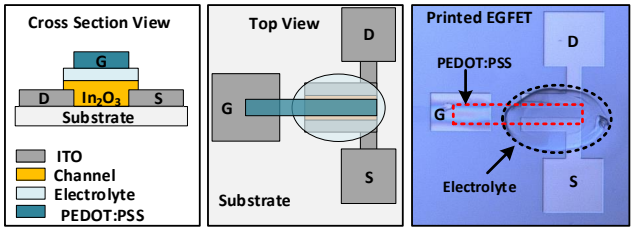
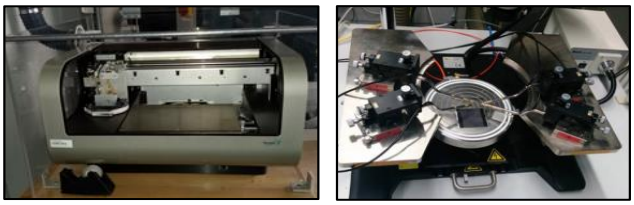


Figure 2: The cross-section, top-view and printed top-gate EGFET (channel width $W = 200\,\mu m$ and length $L = 40\,\mu m$).



Dimatix Materials Printer DMP-2831 **Probe Station**

Figure 3: The Dimatix materials printer and probe station we used for printing and characterization of EGFET based circuits, respectively.

also describe the standard cell libraries we developed for these technologies - to the best of our knowledge, these are the first synthesis and physical design ready standard cell libraries for any low voltage printed technology.

3.1. Electrolyte-Gated Field-Effect Transistors (EGFET) Technology: Overview

Our electrolyte-gated field effect transistors use inorganic semiconducting inks and replace the dielectric with a solid composite electrolyte[12]. Since electrolyte gating leads to high gate capacitance [37], it can drastically reduce the supply voltage ($< 1\,V$) [11, 25, 109, 27, 26]. Additionally, the printed inorganic oxide semiconductors for the channel material offer high field-effect mobility [37]. The typical threshold voltage (V_{th}) of EGFET is 0.17 V which makes it a promising candidate for battery-powered applications. The EGFET is prepared on glass-substrate by printing the channel material (In_2O_3) between the indium tin oxide (ITO) source and drain electrodes. The primary reason to use In_2O_3 is its higher intrinsic mobility ($126 cm^2$/Vs for In2O3 vs $47.1 cm^2$/Vs for ZnO and $96.4 cm^2$/Vs for Tin-Oxide). Next, electrolyte is inkjet printed as gate isolation over the channel region. Finally, the top-gate material PEDOT:PSS[2] is printed on top of the electrolyte. The cross-section view of the EGFET with the materials stack, top-view, and an optical picture of the printed EGFET are shown in Figure 2. In our work, all printed layers are printed using Dimatix DMP-2831 materials printer (Figure 3).

In EGFET technology, only n-type devices are available as no reliable p-type inkjet printed EGFET has been realized yet [35]. This prohibits the use of Pseudo-CMOS as NMOS-based Pseudo-CMOS consumes excessive power compared to transistor-resistor logic. The circuits are hence fabricated in transistor-resistor logic where the resistor is used for the pull-up logic while EGFET is used for the pull-down logic. Typical EGFET channel length is 60um; we can scale down to 10um (<5um using printers such as Ceradrop F-Series , but start seeing short-channel effects. Measured yield for our EGFET devices is 90-99%.

3.1.1. Standard Cell Library for EGFET The published work on standard cell libraries for EGFET-printed technology [86, 71, 87] focuses only on combinational logic gates (NOT, NAND and NOR). Since these libraries do not have sequential logic gates (latch and flip-flop) and tri-state buffers, we cannot use the existing libraries for synthesis or physical design of microprocessors. Nor can these libraries be used for the architectural design space exploration and/or to perform optimization on printed microprocessors. Also, in the existing libraries, the compact models for EGFET are not based on purely physical parameters[86, 71].

We developed a EGFET standard cell library containing NOT (INVX1), 2-input NAND (NAND2X1), 2-input NOR (NOR2X1), 2-input AND (AND2X1), 2-input OR (OR2X1), 2-input XOR (XOR2X1), 2-input XNOR (XNOR2X1),SR-Latch (LATCHX1), D Flip-Flop (DFFX1), D Flip-Flop with asynchronous reset (DFFNRX1) and tri-state buffer (TSBUFX1) cells.[3] To characterize delay and power, we enhanced previously published EGFET compact models using measurement proven capacitance values (measured from the printed EGFETs) - [31, 30] describe how to extract and accurately model the gate-capacitance using measured data. These models are then used to characterize standard cells. The delay and power values of the characterized cells are verified with measured delay and power values of the printed logic circuits, whenever applicable[4]. Additionally, the layout of the missing sequential gates were drawn and added in the PDK. Typical characteristics of all logic gates are reported in the Table 2. Of particular note is the high overhead of DFF due to its implementation in transistor-resistor logic. This overhead impacts several architectural decision for rinted microprocessors (Section 5).

3.2. Carbon Nanotube (CNT) Thin-Film Transistor Technology: Overview

Carbon nanotube (CNT) thin-film transistor (TFT) is a promising candidate for high-performance printed electronics due to high field-effect mobility, mechanical flexibility and compatibility with low cost printing processes [45]. However, it suffers from low device yield and mismatching between the p- and n-type TFTs [67]. As a result, usually p-type TFTs are used to design circuits in the CNT-TFT technology. The performance characteristics of the CNT-TFT based circuits are improved through pseudo-CMOS [50] design which decreases the leakage power and improves the symmetry between the rise and fall delays of the logic gates. Multiple digital and analog circuits based on CNT-TFT are reported in the litera-

[2] poly(3,4-ethylenedioxythiophene) polystyrene sulfonate

[3] We also developed an X4 library; however, we perform all analysis in this paper using X1 library due to lower leakage

[4] We printed and measured (Figure 3) NOT, NAND, NOR, XOR and latch circuits.

Table 2: Characteristics of standard cells for EGFET at $V_{DD} = 1\,V$ and CNT-TFT at $V_{DD} = 3\,V$

Cell Name	Area mm^2		Energy nJ		Rise Delay µs		Fall Delay µs	
	EGFET	CNT	EGFET	CNT	EGFET	CNT	EGFET	CNT
INVX1	0.224	0.002	9.8	0.093	1212	0.058	174	2.9
NAND2X1	0.247	0.003	12.1	10.01	1557	0.088	986	7.99
NOR2X1	0.399	0.003	580	18.61	1830	0.108	904	3.65
AND2X1	0.433	0.005	584.1	18.35	2101	0.171	1284	8.05
OR22X1	0.563	0.005	603	21.33	2040	0.121	1271	4.10
XOR2X1	1.04	0.012	1460	36.7	5474	1.908	4982	5.65
XNOR2X1	1.34	0.014	1510	37.1	6159	2.118	3420	5.97
LATCHX1	0.58	0.006	624	19.55	2643	0.221	942	3.75
DFFX1	1.41	0.018	2360	41.5	6149	3.78	3923	4.19
DFFNRX1	2.77	0.042	3941	50.7	5935	8.61	4453	8.77
TSBUFX1	0.446	0.003	597	19.5	2553	0.109	1004	2.83

ture [67].

3.2.1. Standard Cell Library for CNT-TFT Prior work [97] developed a compact model for the CNT-TFT which has been verified with the measurement data. The Verilog-A model with some circuit examples is also available online [96]. However, no open-source PDK for the CNT-TFT technology is available. We extended the CNT-TFT model to develop a standard cell library for CNT-TFT technology.

The CNT-TFT standard cell library is developed by designing and characterizing the pseudo-CMOS design based logic gates. The library has the same cells as the EGFET standard library. As reported in [67], the typical supply voltage (V_{DD}) for CNT-TFT is 3 V. The area of the standard-cells are estimated by drawing the layout of the CNT-TFT. Typical characteristics of all logic gates in the CNT-TFT standard library are reported in the Table 2. Note that CNT-TFT cells are much smaller, faster, and lower energy than EGFET, but also need high input voltage and high cost for printing (shadow mask vs inkjet for EGFET).

We have open-sourced both EGFET and CNT-TFT standard cell libraries[1]

4. Understanding Characteristics of Existing Microprocessors in Low Voltage Printed Technologies

With the availability of standard cell libraries (Section 3), we are now ready to characterize the area, power and delay characteristics of some existing microprocessors in low voltage printed technologies. Since we aim to target disposable and ultra-low-end applications, which need to be powered by small batteries, we picked four ultra-low-power (ULP) microcontrollers for our characterization: openMSP430, Z80, light8080, and ZPU. The openMSP430 is a synthesizeable 16-bit microcontroller compatible with the Texas Instruments' MSP430 family. The Z80 is a 8-bit microcontroller from Zilog introduced in 1976 (and still in production!)[110] as an embedded processor in devices such as TI-83 and TI-84 series of graphing calculators. light8080 is a low gate count open-source version of Intel 8080. Zylin's ZPU is a 32 bit microprocessor with a stack-based ISA [111].

Table 4 shows the results. We observe that the maximum operating frequency (f_{max}) of the EGFET printed cores is high enough for several printed applications (Table 3) considering their low duty cycle and sampling requirements (e.g., light level sensor, food temperature sensor, alcohol sensor, body temperature sensor, timer, etc.). In order to target other applications, higher performance is needed. CNT-TFT cores can meet the performance requirement for all applications. However, CNT-TFT suffers from high cost (shadow-mask printing vs inkjet-printing for EGFET) and high power. It also needs relatively high input voltage (3 V typical vs 1 V typical for EGFET) which may limit the power sources that can be used.

In general, power consumption of the existing microprocessors in printed technologies is high. Figures 4 and 5 show the potential lifetimes of the four microprocessors for four different printed batteries (e.g., Molex 90 mA printed battery [76], Bluespark 30 mA [102], Zinergy's 12 mA [126] and Bluespark 10 mA [101]). We see that the lifetime for these existing microcontrollers is only a few hours for both printed technologies (less than 2 hours for all the microprocessors for the CPU duty cycle of 1.0). This may be good enough for some applications that have low duty cycle (e.g., blood pressure sensor, odor sensor, trace metal sensor, etc.). However, for other applications that require high uptime (e.g. some pressure sensor, light sensor, humidity sensor, smart bandages, etc., applications), these microprocessors will not be adequate. Also, several printed batteries have maximum power $\leq 30\,mW$, thus the preexisting cores will require multiple batteries to run at nominal frequency.

Area is also prohibitively high for these pre-existing microprocessors, especially in EGFET technology. Microprocessors with much lower gate count may be needed to address the area and power concerns with printed microprocessors.

In fact, area and power concerns are much worse. Programs need to be stored in an instruction memory which itself will consume area and power. Considering that ULP microprocessors typically have a relatively simple ISA, programs may not be compact and, therefore, the overhead of the instruction memory may be large. This is especially true for the stack-based ZPU. Other cores have more complicated ISAs implemented with a large number of controller states, and consequently have a high CPI (Table 4). Later (Section 8) we discuss how some of these preexisting cores exceed 108 J ($30\,mA \times 3.6\,ks \times 1\,V$) energy budget of a printed battery even for simple benchmarks.

Table 5 shows that the area and power overhead of instruction memory is significant when we store the program in a EGFET RAM.[5] Moreover, instruction memory really needs be implemented as a read-only memory (ROM) for most printed applications - we will discuss in Section 6 how to implement

[5] In order to generate programs, we used msp430-gcc compiler for openmsp430 [3], sdcc [4] compiler for Z80 and light8080, and zpugcc toolchain [5] for ZPU

low area and power overhead, non-volatile instruction memory for low voltage printed applications.

5. Exploring Design Space of Low Voltage Printed Microprocessors

In this section, we aim to design low gate count microprocessors that are better suited to the needs of printed applications. requirements of inkjet printed ISAs. We first describe a new ISA designed for inkjet printed cores. We then present results of design space exploration performed around this new ISA. The same ISA is used for evaluation of CNT-TFT cores.

5.1. Tiny Printed ISA

An instruction set architecture for an inkjet printed microprocessor must have certain characteristics. Since printed cells are large (Table 2), the ISA must be implementable with a simple, low gate-count microarchitecture (discouraging use of CISC ISAs that have high gate and DFF count and are difficult to implement in single cycle; this also discourages use of stack-based ISAs that need expensive RAM-based implementation of stack). Since DFFs are expensive (Table 2), the ISA must minimize use of registers (encouraging use of a memory-memory ISA). Since both instruction and data length

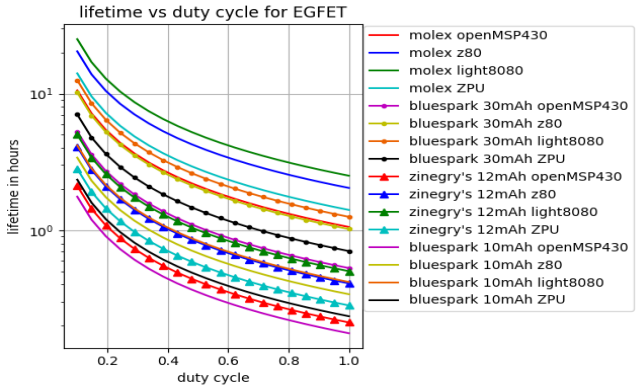


Figure 4: Lifetime vs duty cycle period for EGFET for different printed batteries.

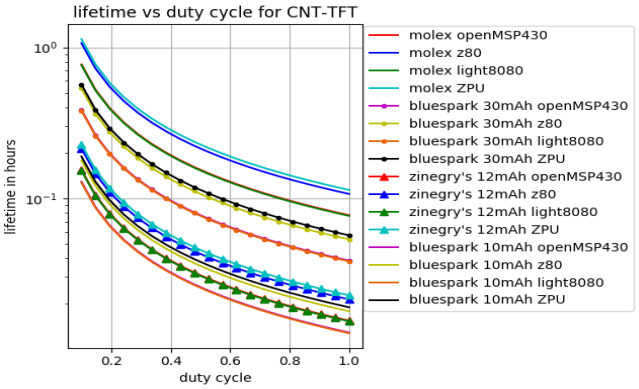


Figure 5: Lifetime vs duty cycle period for CNT_TFT for different printed batteries.

requirements as well as the cost of implementing data and instruction memories can differ in printed systems (Section 6), the ISA should be implementable as a Harvard architecture. Due to the large size and energy cost of memories (Section 6), data and program size will be constrained. So, the ISA does not need to support large address spaces. It must allow compact programs for the target applications. Contrast this against the ISAs of the four cores characterized in the previous section. While Z80 and light8080 ISAs have an excessive number of instructions and addressing modes, ZPU's data width exceeds the precision requirement of many printed applications (Table 3), and its stack-based ISA often necessitates large memories. The openMSP430 is prohibitively large in EGFET, not the least due to an ISA supporting seven addressing modes.

In order to deal with the low gate count and small instruction memory constraints of battery powered inkjet printed systems, we designed a two operand, memory-memory ISA called 'TP-ISA' (Tiny Printed ISA) with a robust set of integer arithmetic and logic operations (Figure 6). The instruction chosen to be included in our ISA are widely used in various applications (including most applications in Table 3). In fact, TP-ISA's arithmetic and logical instructions are a strict subset of those provided by light8080, MSP-430 and Z80, while the non-coalescing ones (see below) are a strict subset of those provided by the 32-bit ZPU. Similar to a stack architecture, a memory-memory ISA minimizes the number of power hungry registers required. But unlike a stack architecture, a memory-memory ISA also allows for an expressive language which leads to smaller program sizes. TP-ISA has three architectural registers: an 8-bit program counter (PC), one or more 8-bit base address registers (BAR), and a 4-bit flags register with (S)ign, (Z)ero, (C)arry out, and o(V)erflow fields. Each TP-ISA instruction is 24-bits wide and contains a 4-bit opcode, 4-bits of control information, and two 8-bit operands, as seen in Figure 6. TP-ISA supports up to 256 words of data memory. Data memory may be of arbitrary width. To determine memory addresses for computation, the least significant bits of each operand are used as offset from the address in a BAR register. The appropriate BAR is selected by the most significant bits of each instruction operand. Additionally, two instructions, 'STORE' and 'SETBAR' treat one of the instruction operands as an immediate value.

The ALU supports most common arithmetic and logic instructions. In order to facilitate data coalescing, add with carry, subtract with borrow, and left and right rotate through carry instructions are supported. A population count instruction was not implemented due to the large number of cells it requires in our PDK relative to its expected utility (26 and 63 cells for 8-bit and 32-bit population counts, respectively). We also did not add shift instructions, only rotate instructions, as the additional area of a barrel shifter is quite large (152 cells and 1109 cells for 8-bit and 32-bit respectively), and shifts do not work gracefully with the ISA's data coalescing scheme.

Table 3: Example applications and their performance/precision requirements

Application	Sample Rate (Hz)	Prec. (bits)	Duty Cycle Period	Application	Sample Rate (Hz)	Prec. (bits)	Duty Cycle Period
Blood Pressure Sensor [81]	<100	8	Hours [22]	Body Temperature Sensor [81]	<1	8	Minutes [58]
Odor Sensor [81]	16-25	8	Minutes [83]	Smart Bandage [78]	<0.01	8	Continuous to Hours [29]
Heart Beat Sensor [81]	<4	1	Seconds [104]	Tremor Sensor [42]	<25	16	Seconds [23]
Pressure Sensor [40]	1-5.5	12	Continuous to Hours [94]	Oral-Nasal Airflow [81]	<25	8	Seconds
Light Level Sensor [81]	<1	16	Continuous to Hours [24]	Perspiration Sensor [61]	<25	16	Minutes [119]
Trace Metal Sensor [61]	25	16	Minutes	Pedometer [82]	<25	1	Seconds [82]
Food Temp. Sensor [81]	<1	16	5 minutes [6]	Timer [53]	1	1	Single Use
Alcohol Sensor [60]	1	8	Single Use [75]	POS Computation [74]	<100	8	Single Use [74]
Humidity Sensor [48]	10	16	Continuous to Hours [93]				

Table 4: Specifications and characteristics of pre-existing CPUs

CPUs	datawidth - Alu width	ISA	CPI	Fmax (Hz) (EGFET@1V/CNT-TFT@3V)	Gate Count (EGFET@1V/CNT-TFT@3V)	Area (cm^2) (EGFET@1V/CNT-TFT@3V)	Power (mW) (EGFET@1V/CNT-TFT@3V)
openMSP430 [39]	16-16	Register based	1-6	4.07/15074	12101/14098	56.38/0.69	124.4/1335.8
Z80 [90] [70]	8-8	Enhanced Intel8080	3-23	7.18/26064	5263/7226	25.28/0.34	76.25/1204
Light8080 [54]	8-8	Intel8080	5-30	17.39/57238	1948/3020	11.15/0.17	41.7/1517
ZPU_small [47]	32-8	Stack-based	4	25.45/43442	2984/3782	15.82/0.21	66.06/1596

Table 5: Instruction memory overhead for EGFET for different benchmarks, A: area in cm^2 and P: power in mW

	Mult		Div		inSort		intAvg		tHold		crc8		dTree	
CPUs	A	P	A	P	A	P	A	P	A	P	A	P	A	P
MSP430	4.3	9.8	4.3	9.8	10	24	6.3	14	5.7	13	7.3	16	31	71
ZPU	8.2	18	30	69	4.9	11	11	25	8.2	18	13	31	44	101
Z80	2.2	5.2	2.9	6.7	2.4	5.6	1.8	4.1	2.6	6	14	33	55	126
light8080	2.2	5.2	2.9	6.7	2.6	6.1	1.8	4.1	2.6	6	14	33	55	126

Instruction Format	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M-Type:	opcode				W	C	A	B	R	address1							S	address2						
ADD	OP-ADD				1	0	0	0	R	address1							S	address2						
ADC	OP-ADD				1	1	0	0	R	address1							S	address2						
SUB	OP-ADD				1	0	1	0	R	address1							S	address2						
CMP	OP-ADD				0	0	1	0	R	address1							S	address2						
SBB	OP-ADD				1	1	1	0	R	address1							S	address2						
AND	OP-AND				1	0	0	0	R	address1							S	address2						
TEST	OP-AND				0	0	0	0	R	address1							S	address2						
OR	OP-OR				1	0	0	0	R	address1							S	address2						
XOR	OP-XOR				1	0	0	0	R	address1							S	address2						
NOT	OP-NOT				1	0	0	0	R	address1							S	address2						
RL	OP-RL				1	0	0	0	R	address1							S	address2						
RLC	OP-RL				1	1	0	0	R	address1							S	address2						
RR	OP-RR				1	0	0	0	R	address1							S	address2						
RRC	OP-RR				1	1	0	0	R	address1							S	address2						
RRA	OP-RR				1	0	1	0	R	address1							S	address2						
S-Type:	opcode				W	3'b0			R	address1							immediate							
STORE	OP-STORE				1	0	0	0	R	address1							immediate							
SET-BAR	OP-BAR				0	0	0	0	x	ptr address							immediate							
B-Type:	opcode				4'b0001				R	address1							4'b0				bmask			
BR	OP-BR				0	0	0	1	R	address1							0	0	0	0	bmask			
BRN	OP-BR				0	0	1	1	R	address1							0	0	0	0	bmask			

Figure 6: Tiny printed ISA (TP-ISA) Instructions

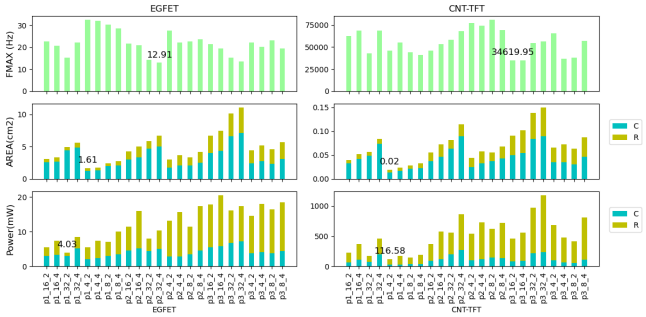


Figure 7: f_{max} in Hz, Area in cm^2 and Power in mW. Cores are described as pP_D_B where P is the number of pipeline stages, D is the datawidth, and B is the number of base address registers, C: Combinational, R: Registers.

5.2. Design Space Exploration

With the ISA set, we performed design space exploration across three dimensions: datawidth, pipeline depth, and BAR count. We synthesized cores with data and ALU widths of 4, 8, 16, and 32 bits, with 1, 2, and 3 stage pipelines, and with 2 and 4 BARs using Synopsys Design Compiler 2019. In all versions, BAR[0] is set to zero.

Figure 7 shows power, area, and maximum frequency of TPISA cores. We see that TP-ISA enables low gate count implementations. The largest TP-ISA core (a 32-bit, 3-stage pipelined core with 4 BARs) is smaller than the smallest pre-existing core (the 8-bit light8080). The smallest 8-bit TP-ISA core is 5.2x smaller than the light8080.

Despite their small number of pipeline stages, the TP-ISA cores have relatively high frequencies, with the fastest TP-ISA core (p1_4_4) running over 38% faster than the fastest pre-existing core (light8080), and the slowest TP-ISA core (p3_32_2) running faster than both the Z80 and openMSP430

cores. CPI numbers for the TP-ISA cores are also better, with worst case CPI being equal to the number of pipeline stages (stalls are used to resolve data and control hazards).

The power consumed by the TP-ISA cores is significantly less than the power consumed by the pre-existing cores, despite dynamic power being proportional to frequency. At under 7 mW, the single-cycle 8-bit TP-ISA core consumes under 20% of the power consumed by light8080 while boasting a far higher IPS. Similarly, the best 16-bit TP-ISA core consumes 11.4% of the power consumed by the Z80 core with, once again, a far higher IPS. The same pattern holds for 32-bit cores as the best 32-bit TP-ISA core consumes only 7.4% of the power of the ZPU-Small core.

We also observe that registers consume a significant fraction of overall area and power. This directly follows from the high cost of sequential logic cells compared to combinational logic cells (Table 2) in printed technologies.

6. Memory Design for Printed Microprocessors

As observed in Section 4, RAM-based memory for printed microprocessors could be expensive. While data memory sizes tend to be small for printed applications, a simple ISA for printed microprocessors can increase code size and, therefore, area and power of instruction memory. Instruction memory also has non-volatility requirements.

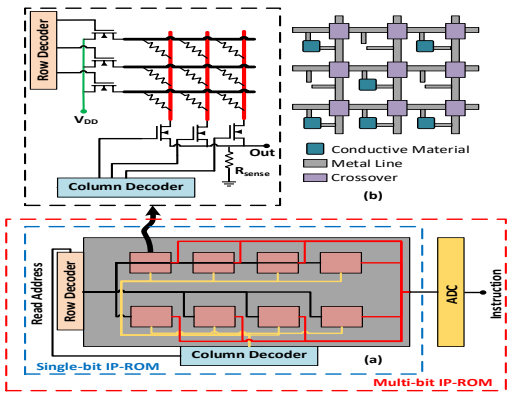


Figure 9: (a) Inkjet printed resistor based Read Only Memory architecture and (b) layout of the crossbar architecture.

Our read-only instruction memory for EGFET-based processors is based on a crossbar architecture (Figure 9) where the cross-points are shorted by printing a conductive material (such as PEDOT:PSS) to represent a bit-value. A sensing resistor is used in each sub-block to read the cross-point value. The voltage drop on sensing resistor defines the cross-point resistance value. The row and column decoders are shared among all sub-blocks (each memory block has 8 sub-blocks). Additionally, the sensing resister is also shared among all columns to further reduce the area.

On an instruction fetch, the read address is decoded by the row and column decoders. The cross-point, in each sub-block, is read based on the read address. If the cross-point is shorted then cross-point resistance is very low compared to the sensing resistor and maximum voltage drop (logic HIGH) is read at the sensing resistor. On the other hand, if the cross-point is open (no conductive material printed), then the minimum voltage drop (logic LOW) is sensed as the non-shorted cross-point resistance is much higher compared to the resistance of the sensing resistor. The output voltage level from each sub-block becomes the instruction for the processor. Prior work [79] on inkjet printing based programmable instruction memory is based on a NOR architecture where a 4-to-16 line address decoder is used to select a row in the printable write-once-read-many times (WORM) memory. Our proposed ROM has an advantage in terms of the area as it requires only one transistor per row and one per column. Additionally the proposed crossbar architecture is more dense, compared to the WORM memory, as only passive structures are required to read the cross-point value. The instruction memory reported in [79] requires 815 transistors (+189 additional transistors to support programming and interface) with the total area of 62.1 mm^2. For the same memory size (16×9), our proposed architecture requires 9 sub-blocks with 16 rows and 1 column per block summing up to 220 transistors and 52 pull-up resistors. The area of such memory is 20.42 mm^2 which is roughly $\frac{1}{3}$ the area compared to the ROM architecture proposed in [79].

Table 6: Characteristics of EGFET Memory Devices, 2-bit ROM: Printed-Dot encodes 2 bits, 4-bit ROM: Printed-Dot encodes 4 bits.

Component	Area [mm^2]	Active Power [µW]	Static Power [µW]	Delay [ms]
1-bit RAM	0.84	16	3.23	2.5
1-bit ROM	0.05	2.77	0.362	1.03
2-bit ROM	0.057	1.87	0.362	1.56
4-bit ROM	0.087	3.01	0.362	3.1
2-bit ADC	3.76	56.8	4.5	5.63
4-bit ADC	25.4	306	22.5	13.8

The density of the proposed instruction ROM can be increased by storing a multi-bit value in a printed dot (multi-level cell - MLC). This can be achieved by varying the geometry of the conductive material which will eventually change the resistance of the material. An analog-to-digital converter (ADC) is used to distinguish among the different voltage values a cross-point read could produce. We have successfully printed instruction ROMs where each cross-point can represent up to four bits. Table 6 lists the characteristics of our EGFET-printed instruction ROM. Note over an order of magnitude benefit from the proposed ROM design in terms of area over a RAM-based memory - this benefit is in addition to the non-volatility benefits of the proposed design.

We have also designed an analogous CNT-TFT version of instruction ROM where Logic HIGH is realized by fabricating a CNT-TFT with drain and gate terminal combined (also known as a diode connected transistor), while logic LOW is realized by having an open path in the memory matrix.

The data memory is realized using a conventional static random-access memory (SRAM) architecture. The EGFET

based single-bit SRAM cell characteristics are described in Table 6.

7. Program-specific ISA

Despite the simplicity of the TP-ISA cores, they are still unnecessarily large. For many programs, an eight bit address space is excessive for instruction memory, data memory, or both. This is an inefficiency which is unavoidable in silicon based hardware (since the cost of manufacturing a program-specific microprocessor is prohibitive), but can be dealt with in printed hardware by printing program-specific hardware.

Since the number of static instructions, N, is known at print time, the program counter can be reduced from eight bits to $\lceil \log_2 N \rceil$ bits. Similarly, since data memory usage is known at print time, the BAR registers may be reduced to $\lceil \log_2 D \rceil$ bits where D is the number of memory addresses used in the program, or even removed entirely if unused. Further, flags are only useful if they are used, and their usage is known at print time. Thus unused bits of the flag register may be removed. These three optimizations, easily automatable through static program analysis, help alleviate the area and power consumed by architectural registers and also reduce the amount of combinational logic (e.g. BAR select muxes and address resolution logic may be removed).

We can also reduce the size of the instruction ROM by targeting the size of the instruction operands. In the M-Type instruction format (Figure 6), the address1 and address2 fields need not be larger than the minimum size needed to hold the largest address offset used. The same is true for the address and immediate values of the S-Type instructions. In B-Type instructions, the second operand must be at least as many bits as the number of flag register bits used. Since the TP-ISA cores implement a Harvard architecture with fixed size instruction words, this change has no significant impact on the PC or instruction fetch hardware (other than narrowing its width).

Table 7 shows the size and number of architectural registers used by benchmark specific variants of TP-ISA. The versions of the analyzed benchmarks are those meant to run on a core whose native data width is the same as the programs data width (i.e. mult8 for an 8-bit core), and which were originally written for the 2 BAR ISA variant. The table reveals that for each benchmark, the base TP-ISA has a large amount of unused architectural state. Section 8 shows the overall power, area, and performance benefits of a program-specific ISA.

Note that there is considerable amount of previous work on customizing hardware for a given application [56, 52, 107]. Application-specific instruction processors (ASIPs) [19], for example, add custom instructions to the base ISA (or sometimes pruning instructions from the base ISA). Much of that work can be leveraged for optimization of program-specific printed microprocessors with the added benefit that low fabrication cost of printed hardware allows a much more fine-grained tuning for a given program (e.g., in the above discussion, we perform a fine-grained customization of the number and size of registers and operands).

Table 7: Size and number of architectural registers in Application Specific TP-ISA variants.

Benchmark	PC Size	BAR Size	# of BARs	# of flags	Instruction Size
CRC8	5	N/A	0	1	16 bits
div	5	N/A	0	2	20 bits
dTree	8	N/A	0	1	24 bits
inSort	5	5	1	2	18 bits
intAvg	6	N/A	0	0	18 bits
mult	4	N/A	0	1	20 bits
tHold	5	5	1	1	20 bits

8. Application-level Analysis of Printed Microprocessors

Now that we have a memory design for printed microprocessors, we are ready to perform application-level evaluations where instructions are stored in the proposed ROM which is just large enough to store exactly as many static instructions as exist in the program. Data memory is implemented as a RAM which contains exactly as many entries as are required by the application (application data memory usage is discernible from static analysis of the code).

Our benchmarks include multiply, divide, inSort, intAvg, threshold, CRC8, and a decision tree. These benchmarks are taken from [121], except for the last which is new. The inSort, intAvg, and threshold benchmarks act on arrays of 16 data words stored in memory. The CRC8 kernel acts on a 16 byte data stream. For each benchmark other than CRC8, we evaluated 8-bit, 16-bit, and 32-bit versions of the benchmark. The decision tree threshold parameters are effectively hard-coded into the program instructions, meaning they do not exist in data memory. We designed the decision tree program to use all 256 instruction words without data coalescing instructions. Thus the 32-bit version of the benchmark is not executed by 16-bit cores, the 16-bit version is not executable by 8-bit cores, etc.

Figure 8 displays benchmark level results for EGFET cores. In the area and energy plots[6], bars are partitioned into four color components which represent the contribution of combinational logic, registers, instruction memory, and data memory to the overall area and energy consumption, respectively. In the execution time plots, the bars are similarly partitioned into color components representing the contribution of core logic, instruction memory, and data memory on execution time. Results are presented only for single cycle cores since our analysis showed that single stage pipelines always outperformed multi-stage pipelines (due to high cost of registers). We evaluate both standard (non-program specific) TP-ISA cores as well program-specific ISA cores.

For each benchmark, the standard (non-program specific) TP-ISA cores whose datawidth is equal to the width of the

[6]The average simulated activity factor for our cores, required for computing energy calculation is 0.88calculated by Design Compiler.

data outperform all other standard cores in terms of energy and delay (e.g. the best performing core in 32-bit multiplication is a 32-bit core). However, the data coalescing instructions allow smaller than optimal cores to perform reasonably close to the best cores in energy while maintaining a smaller area. It is reasonable to believe that, given a TP-ISA program which uses mixed width data, the smaller core will outperform the larger core.

For each benchmark, the program-specific ISA core consumes less energy than all other cores, and uses less area than all other cores which support the same datawidth. The energy margin gained by using the application-specific core is benchmark dependent, but is generally substantial (2.59x-1.16x) on 8-bit benchmarks since the standard 8-bit cores have a higher ratio of register to combinational logic elements than do 16-bit and 32-bit cores.

Table 8 shows the number of times each benchmark can be executed if powered by a 30 mA printed battery on the most energy efficient standard TP-ISA core and the program-specific ISA core. The results in Table 8 suggest that inkjet printed EGFET cores can be used to effectively target applications with duty cycles similar to the ones in Table 3, even after the energy cost of attached printed sensors [93, 94, 92] is considered.

While the presented results are for 1-bit instruction ROM, using each crosspoint to represent multiple bits also has benefits. The effect of this optimization is seen in Figure 8 (dTree-ROMopt), which shows the area, energy, and delay characteristics of the decision tree benchmark while using an MLC (2-bit) instruction ROM. With 256 instruction words, using a 2-bit MLC ROM cell reduces instruction memory area by almost 30%, with less than 1% increase in energy consumption per iteration.

Benchmark level results of existing cores (not shown) further reveal that they are infeasible in inkjet printed EGFET. The light8080 core takes 44.6 s and 3.66 J to execute an 8-bit multiply, which is more than an order of magnitude worse than the best TP-ISA core (but still better than Z80 and ZPU). For 16-bit insertion sort, light8080, Z80, and ZPU have execution times exceeding 1000 s, and, in the case of Z80 and ZPU, consume more energy than a 30 mA battery supplying 1 V can store. Benchmark-level results (not shown) reveal CNT-TFT TP-ISA cores, as expected, have orders of magnitude better performance and energy consumption than EGFET cores. Thus, whenever cost allows (recall that shadow mask-based CNT-TFT is considerably more expensive than inkjet-printed EGFET), CNT-TFT cores may be useful for targeting applications with high duty cycles, where EGFET cores may either be too slow to support the application, or consume too much energy. CNT-TFT execution times are dominated by 302 µs ROM access latencies, indicating a more complex microarchitecture including an instruction cache may be appropriate for CNT-TFT. However, as in the core-level results, CNT-TFT power consumption at nominal frequency exceeds the output of currently available printed batteries. Thus reducing the CNT-TFT cores clock period to match the instruction ROM latency may be more appropriate. We also observe that CNT-TFT cores benefit more from program-specific ISA than EFGET cores due to the very high cost of CNT-TFT registers relative to logic (Table 2).

Table 8: Maximum program iteration count for the most efficient standard EGFET TP-ISA core (STD) and program-specific (PS) cores for each benchmark, When cores are powered by a 1 V, 30 mA h battery. Power consumption incorporates core, ROM, and RAM power.

Benchmark	8-bit		16-bit		32-bit	
	STD	PS	STD	PS	STD	PS
crc8	158	367				
dTree	12,087	20,203	7797	10,997	3865	4257
div	2871	6404	1005	1660	260	346
inSort	237	299	139	160	62	66
intAvg	4495	7987	2646	3480	1219	1427
mult	3727	9689	1268	2512	362	516
tHold	5576	6465	3306	3680	1500	1640

9. Summary and Conclusion

Printed electronics holds the promise to meet the needs of disposable, conformal, and ultra-low cost applications. Recent printing technologies have low enough supply voltage that corresponding electronics can be battery-powered. In this paper, we presented the first exploration of the design and optimization space for low voltage printed microprocessors. To enable this exploration, we first developed the standard cell libraries for EGFET and CNT-TFT printed technologies - these are the first synthesis and physical design ready standard cell libraries for any low voltage printing technology. We then presented an area, power, and delay characterization of several off-the-shelf low gate count microprocessors (Z80, light8080, ZPU, and openMSP430) in EGFET and CNT-TFT technologies. Our characterization showed that while several printing applications can be feasibly targeted by battery-powered printed microprocessors, significant area and power reduction is needed. We performed a design space exploration of printed microprocessor architectures over multiple parameters - datawidths, pipeline depth, etc. We showed that the best cores outperform pre-existing cores by at least one order of magnitude in terms of power and area. Finally, we presented printing-specific optimizations that can be used to further improve area and power characteristics of low voltage battery-compatible printed microprocessors. Program-specific ISA, for example, improves core power, and area by up to 4.18x and 1.93x respectively, and benchmark energy consumption by up to 2.59x. Crosspoint-based instruction ROM outperforms a RAM-based design by 5.77x, 16.8x, and 2.42x respectively in terms of power, area, and delay.

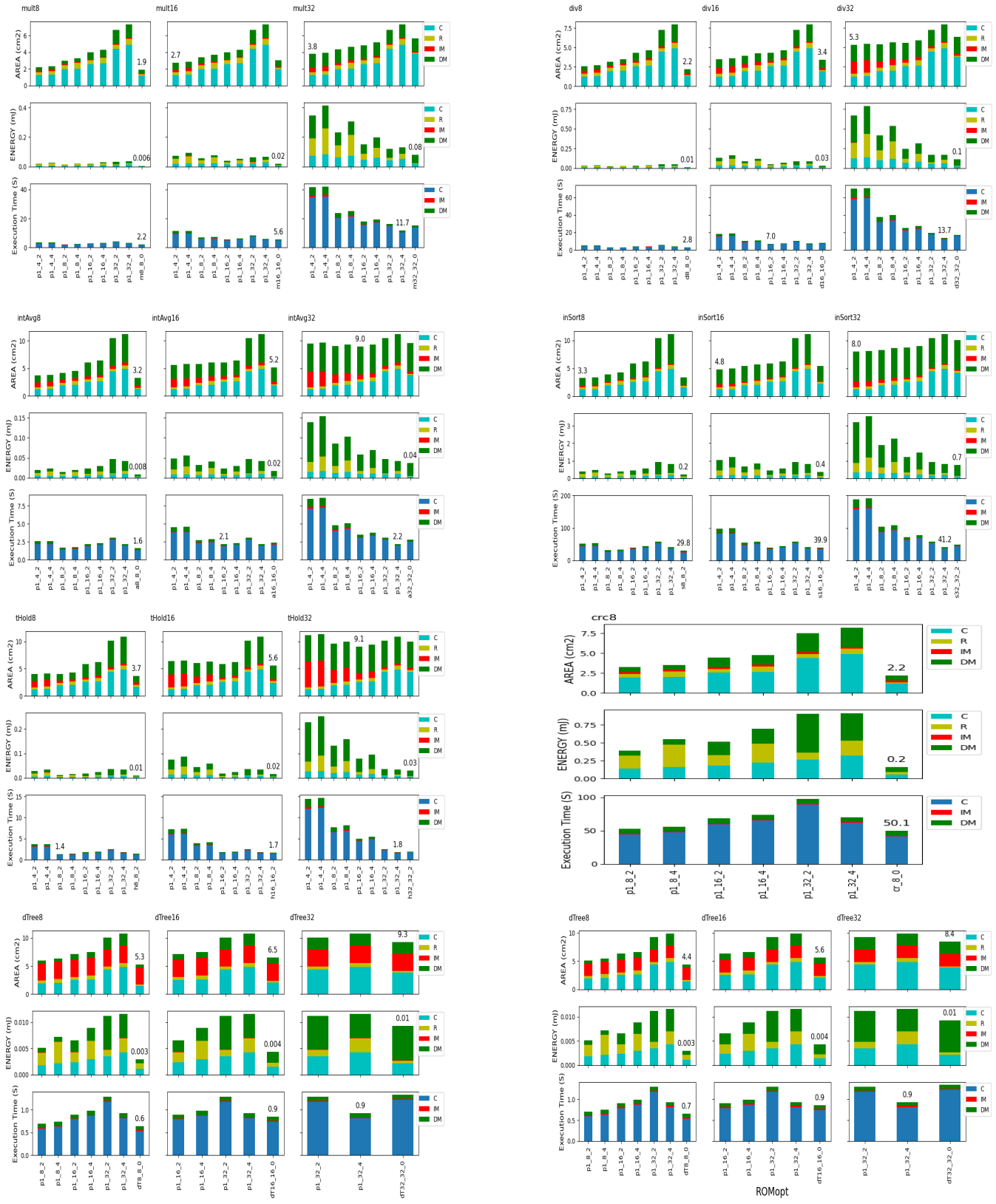


Figure 8: **Benchmarks: Area cm^2, Energy mJ and Execution Time Sec for different cores. Cores are described as pP_D_B where P is the number of pipeline stages, D is the datawidth, and B is the number of base address registers. C: Combinational, R: Registers, IM: Instruction Memory, DM: Data Memory. The rightmost bars in each subfigure represent the program specific system.**

References

[1] https://www.alibaba.com/trade/search?fsb=y&IndexArea=product_en&CatId=&SearchText=java+card.

[2] The amazing 1 dollar microcontroller. https://jaycarlson.net/microcontrollers/.

[3] MSP430_GCC COMPILER TOOLCAHIN. http://www.ti.com/tool/MSP430-GCC-OPENSOURCE.

[4] SDCC COMPILER TOOLCAHIN FOR Z80. https://sourceforge.net/p/sdcc/wiki/z80/.

[5] ZPU_GCC COMPILER TOOLCAHIN. https://github.com/zylin/zpugcc.

[6] *USDA FSIS Directive 7110.3 Rev 1: Time/Temperature Guidelines for Cooling Heated Products*.

[7] Alibaba. 330ml amber glass beer bottle. https://www.alibaba.com/product-detail/330ml-amber-glass-beer-bottle_60161793256.html?spm=a2700.7724857.normalList.1.7b1e7639e26pYC.

[8] Alibaba. Aluminum can for drink/beer/soda. https://www.alibaba.com/product-detail/Aluminum-can-for-drink-soda-beer_60449318643.html?spm=a2700.7724857.normalList.21.26c53bdaEE24NZ&s=p.

[9] Alibaba. Surgical elastic medical conforming 100% cotton gauze bandage. https://www.alibaba.com/product-detail/Surgical-elastic-medical-conforming-100-cotton_60505226320.html?spm=a2700.7724838.2017115.87.7cc91713rWJVYP.

[10] Jinisha Bhanushali, Piyush Dinde, and Shreya Chakraborty. Internet of things: Machine to machine communication with emphasis on role of rfid and nfc. *International Journal of Scientific Engineering Research*, 6(11):779–785, Nov 2015.

[11] Gabriel Cadilha Marques, Suresh Kumar Garlapati, Simone Dehm, Subho Dasgupta, Horst Hahn, Mehdi Tahoori, and Jasmin Aghassi-Hagmann. Digital power and performance analysis of inkjet printed ring oscillators based on electrolyte-gated oxide electronics. *Applied Physics Letters*, 111(10):102103, 2017.

[12] Gabriel Cadilha Marques, Dennis Weller, Ahmet Turan Erozan, Xiaowei Feng, Mehdi Tahoori, and Jasmin Aghassi-Hagmann. Progress report on "from printed electrolyte-gated metal-oxide devices to circuits". *Advanced Materials*, page 1806483, 2019.

[13] Jordi Carrabina. TDK4PE/ASPEC-TDK DESIGN KIT EDA TOOLS. http://www.cnm.es/~icas/PDK/main.html, 2013.

[14] Joseph Chang, Xi Zhang, Tong Ge, and Jia Zhou. Fully printed electronics on flexible substrates: High gain amplifiers and dac. *Organic Electronics*, 15(3):701–710, 2014.

[15] Joseph S Chang, Antonio F Facchetti, and Robert Reuss. A circuits and systems perspective of organic/printed electronics: Review, challenges, and contemporary and emerging design approaches. *IEEE Journal on emerging and selected topics in circuits and systems*, 7(1):7–26, 2017.

[16] Ting-Jung Chang, Zhuozhi Yao, Paul J Jackson, Barry P Rand, and David Wentzlaff. Architectural tradeoffs for biodegradable computing. In *Proceedings of the 50th Annual IEEE/ACM International Symposium on Microarchitecture*, pages 706–717. ACM, 2017.

[17] Kwang-Ting (Tim) Cheng and Tsung-Ching Huang. What is flexible electronics? *SIGDA Newsl.*, 39(4):1–1, April 2009.

[18] Seungjun Chung, Seul Ong Kim, Soon-Ki Kwon, Changhee Lee, and Yongtaek Hong. All-inkjet-printed organic thin-film transistor inverter on flexible plastic substrate. *IEEE electron device letters*, 32(8):1134–1136, 2011.

[19] Jason Cong, Jason Cong, Yiping Fan, Guoling Han, and Zhiru Zhang. Application-specific instruction generation for configurable processor architectures. In *Proceedings of the 2004 ACM/SIGDA 12th international symposium on Field programmable gate arrays*, pages 183–189. ACM, 2004.

[20] Júlio C Costa, Filippo Spina, Pasindu Lugoda, Leonardo Garcia-Garcia, Daniel Roggen, and Niko Münzenrieder. Flexible sensors—from materials to applications. *Technologies*, 7(2):35, 2019.

[21] Zheng Cui. *Printed electronics: materials, technologies and applications*. John Wiley & Sons, 2016.

[22] Kazuo Eguchi, Sujith Kuruvilla, Gbenga Ogedegbe, William Gerin, Joseph E Schwartz, and Thomas G Pickering. What is the optimal interval between successive home blood pressure readings using an automated oscillometric device? *Journal of Hypertension*, 27(6):1172–1177, 2009.

[23] Rodger J Elble and James McNames. Using portable transducers to measure tremor severity. *Tremor and Other Hyperkinetic Movements*, 6, 2016.

[24] enocean. Light level sensor – ceiling mounted. https://www.enocean.com/en/products/enocean_modules_902mhz/light-level-sensor-ells-oem/user-manual-pdf.

[25] Ahmet Turan Erozan, Gabriel Cadilha Marques, Mohammad Saber Golanbari, Rajendra Bishnoi, Simone Dehm, Jasmin Aghassi-Hagmann, and Mehdi B Tahoori. Inkjet-printed egfet-based physical unclonable function—design, evaluation, and fabrication. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 26(12):2935–2946, 2018.

[26] Ahmet Turan Erozan, Guan Ying Wang, Rajendra Bishnoi, Jasmin Aghassi-Hagmann, and Mehdi B Tahoori. A compact low-voltage true random number generator based on inkjet printing technology. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 2020.

[27] Ahmet Turan Erozan, Dennis D Weller, Farhan Rasheed, Rajendra Bishnoi, Jasmin Aghassi-Hagmann, and Mehdi B Tahoori. A novel printed look-up table-based programmable printed digital circuit. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 2020.

[28] F. Farabullini, F. Lucarelli, I. Palchetti, G. Marrazza, and M. Mascini. Disposable electrochemical genosensor for the simultaneous analysis of different bacterial food contaminants. *Biosensors and Bioelectronics*, 22(7):1544 – 1549, 2007.

[29] Muhammad Fahad Farooqui and Atif Shamim. Low cost inkjet printed smart bandage for wireless monitoring of chronic wounds. *Scientific reports*, 6:28949, 2016.

[30] Xiaowei Feng, Gabriel Cadilha Marques, Farhan Rasheed, Mehdi B Tahoori, and Jasmin Aghassi-Hagmann. Non-quasi-static capacitance modeling and characterization for printed inorganic electrolyte-gated transistors in logic gates. *IEEE Transactions on Electron Devices*, 2019. (Accepted).

[31] Xiaowei Feng, Christian Punckt, Gabriel Cadilha Marques, Michael Hefenbrock, Mehdi B Tahoori, and Jasmin Aghassi-Hagmann. Impact of intrinsic capacitances on the dynamic performance of printed electrolyte-gated inorganic field effect transistors. *IEEE Transactions on Electron Devices*, 66(8):3365–3370, 2019.

[32] Pedro Ferreira, Ricardo Martinho, and Dulce Domingos. Iot-aware business processes for logistics: limitations of current approaches. 2010.

[33] Christine Frederickx, François Verheggen, and Eric Haubruge. Biosensors in forensic sciences. *Biotechnologie, Agronomie, Société et Environnement*, 15(3):449–458, 2011.

[34] Wei Gao, Sam Emaminejad, Hnin Yin Yin Nyein, Samyuktha Challa, Kevin Chen, Austin Peck, Hossain M. Fahad, Hiroki Ota, Hiroshi Shiraki, Daisuke Kiriya, Der-Hsien Lien, George A. Brooks, Ronald W. Davis, and Ali Javey. Fully integrated wearable sensor arrays for multiplexed in situ perspiration analysis. *Nature*, 529:509 EP –, Jan 2016.

[35] Suresh Kumar Garlapati, Tessy Theres Baby, Simone Dehm, Mohammed Hammad, Venkata Sai Kiran Chakravadhanula, Robert Kruk, Horst Hahn, and Subho Dasgupta. Ink-jet printed cmos electronics from oxide semiconductors. *Small*, 11(29):3591–3596, 2015.

[36] Suresh Kumar Garlapati, Mitta Divya, Ben Breitung, Robert Kruk, Horst Hahn, and Subho Dasgupta. Printed electronics based on inorganic semiconductors: From processes and materials to devices. *Advanced Materials*, 30(40):1707600, 2018.

[37] Suresh Kumar Garlapati, Nilesha Mishra, Simone Dehm, Ramona Hahn, Robert Kruk, Horst Hahn, and Subho Dasgupta. Electrolyte-gated, high mobility inorganic oxide transistors from printed metal halides. *ACS applied materials & interfaces*, 5(22):11498–11502, 2013.

[38] Inc Gartner. Gartner says worldwide wearable device sales to grow 26 percent in 2019. https://www.gartner.com/en/newsroom/press-releases/2018-11-29-gartner-says-worldwide-wearable-device-sales-to-grow- .

[39] Olivier Girard. OPENMSP430. https://opencores.org/projects/openmsp430, 2015.

[40] Willem Schwalb Yongwei Wang Yi Chen Yue Tang Jye Si Bijan Shirinzadeh Gong, Shu and Wenlong Cheng. A wearable and highly sensitive pressure sensor with ultrathin gold nanowires. *Nature communications*, 2014.

[41] S. Gradl, P. Kugler, C. Lohmüller, and B. Eskofier. Real-time ecg monitoring and arrhythmia detection using android-based mobile devices. In *2012 Annual International Conference of the IEEE Engineering in Medicine and Biology Society*, pages 2452–2455, Aug 2012.

[42] Giuliana Grimaldi and Mario Manto. Neurological tremor: sensors, signal processing and emerging applications. *Sensors (Basel, Switzerland)*, 10(2):1399–1422, 2010. 22205874[pmid].

[43] Guigang Zhang, Chao Li, Yong Zhang, Chunxiao Xing, and Jijiang Yang. Semanmedical: A kind of semantic medical monitoring system model based on the iot sensors. In *2012 IEEE 14th International Conference on e-Health Networking, Applications and Services (Healthcom)*, pages 238–243, Oct 2012.

[44] Mingjing Ha, Yu Xia, Alexander A Green, Wei Zhang, Mike J Renn, Chris H Kim, Mark C Hersam, and C Daniel Frisbie. Printed, sub-3v digital circuits on plastic from aqueous carbon nanotube inks. *ACS nano*, 4(8):4388–4395, 2010.

[45] Shu-Jen Han, Jianshi Tang, Bharat Kumar, Abram Falk, Damon Farmer, George Tulevski, Keith Jenkins, Ali Afzali, Satoshi Oida, John Ott, et al. High-speed logic integrated circuits with solution-processed self-assembled carbon nanotubes. *Nature nanotechnology*, 12(9):861, 2017.

[46] Jim Handy. Why are computer chips so expensive. https://www.forbes.com/sites/jimhandy/2014/04/30/why-are-chips-so-expensive/#3ee0f8f479c9.

[47] Øyvind Harboe. ZYLIN ZPU. https://github.com/zylin/zpu, 2009.

[48] J. R. Brent H. Ding J. Yang D. J. Lewis P. O'Brien He, P. and B. Fully printed high performance humidity sensors based on two-dimensional materials. *Nanoscale*, 10:5599–5606, 2018.

[49] Gage Hills, Christian Lau, Andrew Wright, Samuel Fuller, Mindy D Bishop, Tathagata Srimani, Pritpal Kanhaiya, Rebecca Ho, Aya Amer, Yosi Stein, et al. Modern microprocessor built from complementary carbon nanotube transistors. *Nature*, 572(7771):595–602, 2019.

[50] Tsung-Ching Huang, Kenjiro Fukuda, Chun-Ming Lo, Yung-Hui Yeh, Tsuyoshi Sekitani, Takao Someya, and Kwang-Ting Cheng. Pseudo-cmos: A design style for low-cost and robust flexible electronics. *IEEE Transactions on Electron Devices*, 58(1):141–150, 2010.

[51] B Huber, PB Popp, M Kaiser, A Ruediger, and C Schindler. Fully inkjet printed flexible resistive memory. *Applied Physics Letters*, 110(14):143503, 2017.

[52] Brad L Hutchings and Michael J Wirthlin. Implementation approaches for reconfigurable logic applications. In *International Workshop on Field Programmable Logic and Applications*, pages 419–428. Springer, 1995.

[53] Texas Instruments. Nano-power system timer for power gating. http://www.ti.com/lit/ds/symlink/tpl5111.pdf.

[54] Jaruiz. LIGHT8080 DESIGN_NOTES. https://github.com/jaruiz/light8080, 2016.

[55] Ji-chun Zhao, Jun-feng Zhang, Yu Feng, and Jian-xin Guo. The study and application of the iot technology in agriculture. In *2010 3rd International Conference on Computer Science and Information Technology*, volume 2, pages 462–465, July 2010.

[56] Asawaree Kalavade and Edward A Lee. A hardware-software codesign methodology for dsp applications. *IEEE Design & Test of Computers*, (3):16–28, 1993.

[57] Hongki Kang, Rungrot Kitsomboonloha, Kurt Ulmer, Lisa Stecker, Gerd Grau, Jaewon Jang, and Vivek Subramanian. Megahertz-class printed high mobility organic thin-film transistors and inverters on plastic using attoliter-scale high-speed gravure-printed sub-5 μm gate electrodes. *Organic Electronics*, 15(12):3639–3647, 2014.

[58] W R Keatinge, M G Hayward, and N K Mciver. Hypothermia during saturation diving in the north sea. *Bmj*, 280(6210):291–291, Feb 1980.

[59] Bongjun Kim, Seonpil Jang, Michael L Geier, Pradyumna L Prabhumirashi, Mark C Hersam, and Ananth Dodabalapur. High-speed, inkjet-printed carbon nanotube/zinc tin oxide hybrid complementary ring oscillators. *Nano letters*, 14(6):3683–3687, 2014.

[60] Itthipon Jeerapan Somayeh Imani Thomas N. Cho Amay Bandodkar Stefano Cinti Patrick P. Mercier Kim, Jayoung and Joseph Wang. Noninvasive alcohol monitoring using a wearable tattoo-based iontophoretic-biosensing system. *Acs Sensors*, 1:1011–1019, 2016.

[61] William R. de Araujo Izabela A. Samek Amay J. Bandodkar Wenzhao Jia Barbara Brunetti Thiago RLC Paixão Kim, Jayoung and Joseph Wang. Wearable temporary tattoo sensor for real-time trace metal monitoring in human sweat. *Electrochemistry Communications*, 51, 2015.

[62] Hagen Klauk. *Organic electronics: materials, manufacturing, and applications*. John Wiley & Sons, 2006.

[63] Masaya Kondo, Takafumi Uemura, Mihoko Akiyama, Naoko Namba, Masahiro Sugiyama, Yuki Noda, Teppei Araki, Shusuke Yoshimoto, and Tsuyoshi Sekitani. Design of ultraflexible organic differential amplifier circuits for wearable sensor technologies. In *2018 IEEE International Conference on Microelectronic Test Structures (ICMTS)*, pages 79–84. IEEE, 2018.

[64] Ulrike Kraft, Ute Zschieschang, Frederik Ante, Daniel Kälblein, Claudia Kamella, Konstantin Amsharov, Martin Jansen, Klaus Kern, Edwin Weber, and Hagen Klauk. Fluoroalkylphosphonic acid self-assembled monolayer gate dielectrics for threshold-voltage control in low-voltage organic thin-film transistors. *Journal of Materials Chemistry*, 20(31):6416–6418, 2010.

[65] Jimin Kwon, Yasunori Takeda, Kenjiro Fukuda, Kilwon Cho, Shizuo Tokito, and Sungjune Jung. Vertically stacked complementary organic field-effect transistors and logic circuits fabricated by inkjet printing. *Advanced Electronic Materials*, 2(7):1600046, 2016.

[66] M. T. Lazarescu. Design of a wsn platform for long-term environmental monitoring for iot applications. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, 3(1):45–54, March 2013.

[67] Ting Lei, Lei-Lai Shao, Yu-Qing Zheng, Gregory Pitner, Guanhua Fang, Chenxin Zhu, Sicheng Li, Ray Beausoleil, H-S Philip Wong, Tsung-Ching Huang, et al. Low-voltage high-performance flexible digital and analog circuits based on ultrahigh-purity semiconducting carbon nanotubes. *Nature communications*, 10(1):2161, 2019.

[68] W. Lin, M. Lee, and W. Chou. The design and development of a wearable posture monitoring vest. In *2014 IEEE International Conference on Consumer Electronics (ICCE)*, pages 329–330, Jan 2014.

[69] E. N. Mambou, S. M. Nlom, T. G. Swart, K. Ouahada, A. R. Ndjiongue, and H. C. Ferreira. Monitoring of the medication distribution and the refrigeration temperature in a pharmacy based on internet of things (iot) technology. In *2016 18th Mediterranean Electrotechnical Conference (MELECON)*, pages 1–5, April 2016.

[70] CPU User Manual. Z80 family.

[71] G. C. Marques, F. Rasheed, J. Aghassi-Hagmann, and M. B. Tahoori. From silicon to printed electronics: A coherent modeling and design flow approach based on printed electrolyte gated fets. In *2018 23rd Asia and South Pacific Design Automation Conference (ASP-DAC)*, pages 658–663, Jan 2018.

[72] Gabriel Cadilha Marques, Suresh Kumar Garlapati, Debaditya Chatterjee, Simone Dehm, Subho Dasgupta, Jasmin Aghassi, and Mehdi B Tahoori. Electrolyte-gated fets based on oxide semiconductors: Fabrication and modeling. *IEEE Transactions on Electron Devices*, 64(1):279–285, 2016.

[73] Mohammad Mashayekhi, Simon Ogier, Tim Pease, Lluis Teres, and Jordi Carrabina. Comparison of design styles for top-gate bottom-contact otfts. In *2015 Conference on Design of Circuits and Integrated Systems (DCIS)*, pages 1–9. IEEE, 2015.

[74] microsensys GmbH. Telid 281.3dm. https://www.microsensys.de/fileadmin/user_upload/pdf-dateien/ds_sensor-transpond/TELID281M-03.pdf.

[75] Larry Mobley, Brian McMillin, and James Lewis. Vehicle ignition interlock systems having transdermal alcohol sensor, 2006.

[76] Molex. THIN-FILM BATTERY. http://www.literature.molex.com/SQLImages/kelmscott/Molex/PDF_Images/987651-5461.PDF, 2018.

[77] Higinio Mora, David Gil, Rafael Muñoz Terol, Jorge Azorín, and Julian Szymanski. An iot-based computational framework for healthcare monitoring in mobile environments. *Sensors (Basel, Switzerland)*, 17(10):2302, Oct 2017. 28994743[pmid].

[78] P. Mostafalu, W. Lenk, M. R. Dokmeci, B. Ziaie, A. Khademhosseini, and S. R. Sonkusale. Wireless flexible smart bandage for continuous monitoring of wound oxygenation. *IEEE Transactions on Biomedical Circuits and Systems*, 9(5):670–677, Oct 2015.

[79] Kris Myny, Steve Smout, Maarten Rockelé, Ajay Bhoolokam, Tung Huei Ke, Soeren Steudel, Brian Cobb, Aashini Gulati, Francisco Gonzalez Rodriguez, Koji Obata, et al. A thin-film microprocessor with inkjet print-programmable memory. *Scientific reports*, 4:7398, 2014.

[80] Kris Myny, Erik Van Veenendaal, Gerwin H Gelinck, Jan Genoe, Wim Dehaene, and Paul Heremans. An 8-bit, 40-instructions-per-second organic microprocessor on plastic foil. *IEEE Journal of Solid-State Circuits*, 47(1):284–291, 2011.

[81] Bo Zhai A. Olson Anna Reeves Michael Minuth Ryan Helfand Sanjay Pant Todd Austin Nazhandali, Leyla and David Blaauw. Energy optimization of subthreshold-voltage sensor network processors. *Advanced Materials*, pages 197–207, 2005.

[82] NXP. Intelligent motionsensing pedometer. https://www.nxp.com/docs/en/data-sheet/MMA9555L.pdf.

[83] Alvaro Ortiz Pérez, Vera Kallfaß-de Frenes, Alexander Filbert, Janosch Kneer, Benedikt Bierer, Pirmin Held, Philipp Klein, Jürgen Wöllenstein, Dirk Benyoucef, Sigrid Kallfaß, et al. Odor-sensing system to support social participation of people suffering from incontinence. *Sensors*, 17(1):58, 2017.

[84] Paul N Plassmeyer, Kevin Archila, John F Wager, and Catherine J Page. Lanthanum aluminum oxide thin-film dielectrics from aqueous solution. *ACS applied materials & interfaces*, 7(3):1678–1684, 2015.

[85] Eloi Ramon, C Martínez-Domingo, A Alcalde-Aragonés, and Jordi Carrabina. Development of a simple manufacturing process for all-inkjet printed organic thin film transistors and circuits. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, 7(1):161–170, 2016.

[86] F. Rasheed, M. S. Golanbari, G. Cadilha Marques, M. B. Tahoori, and J. Aghassi-Hagmann. A smooth ekv-based dc model for accurate simulation of printed transistors and their process variations. *IEEE Transactions on Electron Devices*, 65(2):667–673, Feb 2018.

[87] Farhan Rasheed, Michael Hefenbrock, Rajendra Bishnoi, Michael BeigI, Jasmin Aghassi-Hagmann, and Mehdi B Tahoori. Predictive modeling and design automation of inorganic printed electronics. In *2019 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 30–35. IEEE, 2019.

[88] Partha P Ray. *Internet of Things based Physical Activity Monitoring (PAMIoT): An Architectural Framework to Monitor Human Physical Activity*, page 32–34.

[89] Brent A Ridley, Babak Nivi, and Joseph M Jacobson. All-inorganic field effect transistors fabricated by printing. *Science*, 286(5440):746–749, 1999.

[90] Manuel Sainz de Baranda y Goñi. ZILOG Z80. https://github.com/zylin/zpu, 2009.

[91] Dirk Schaefer and Wai M. Cheung. Smart packaging: Opportunities and challenges. *Procedia CIRP*, 72:1022 – 1027, 2018. 51st CIRP Conference on Manufacturing Systems.

[92] Bosch Sensortec. 3-axes ultra-low power accelerometer. https://ae-bst.resource.bosch.com/media/_tech/media/datasheets/BST-BMA400-DS000.pdf, 2018.

[93] Bosch Sensortec. Digital humidity, pressure and temperature sensor. https://ae-bst.resource.bosch.com/media/_tech/media/datasheets/BST-BME280-DS002.pdf, 2018.

[94] Bosch Sensortec. Digital pressure sensor. https://ae-bst.resource.bosch.com/media/_tech/media/application_notes/BST-BMP380-HS000.pdf, 2018.

[95] Botao Shao. Fully printed chipless rfid tags towards item-level tracking applications, 2014.

[96] L. Shao. CNT-TFT-VERILOG-A. https://github.com/llshao/CNT-TFT-Verilog-A, 2018.

[97] Leilai Shao, Tsung-Ching Huang, Ting Lei, Zhenan Bao, Raymond Beausoleil, and Kwang-Ting Cheng. Compact modeling of carbon nanotube thin film transistors for flexible circuit design. In *2018 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 491–496. IEEE, 2018.

[98] Leilai Shao, Tsung-Ching Huang, Ting Lei, Zhenan Bao, Raymond Beausoleil, and Kwang-Ting Cheng. Process design kit for flexible hybrid electronics. In *Proceedings of the 23rd Asia and South Pacific Design Automation Conference*, pages 651–657. IEEE Press, 2018.

[99] Ravina Singh, Eric Singh, and Hari Singh Nalwa. Inkjet printed nanomaterial based flexible radio frequency identification (rfid) tag sensors for the internet of nano things. *RSC Advances*, 7(77):48597–48630, 2017.

[100] Robert Sobot. Implantable technologyhistory, controversies, and social implications. *IEEE TEchnology and SocIETy MagazInE*, page 35–45, Dec 2018.

[101] Blue Spark. Blue spark 10mah battery.

[102] Blue Spark. Blue spark 30mah battery.

[103] Vivek Subramanian, Josephine B Chang, Alejandro de la Fuente Vornbrock, Daniel C Huang, Lakshmi Jagannathan, Frank Liao, Brian Mattis, Steven Molesa, David R Redinger, Daniel Soltman, et al. Printed electronics for low-cost electronic systems: Technology status and application development. In *ESSCIRC 2008-34th European Solid-State Circuits Conference*, pages 17–24. IEEE, 2008.

[104] Harold Thorgersen. Heartbeat monitor for wearing during exercise, 2000.

[105] EE Times. Starting all over again on plastic: Arm. https://www.eetimes.com/document.asp?doc_id=1328399, 2015.

[106] IDC Company USA. The growth in connected iot devices is expected to generate 79.4zb of data in 2025, according to a new idc forecast.

[107] Frank Vahid. The softening of hardware. *Computer*, 36(4):27–34, 2003.

[108] Wai Lee and A. Sharma. Smart sensing for iot applications. In *2016 13th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, pages 362–364, Oct 2016.

[109] Dennis Weller, Gabriel Cadilha Marques, Jasmin Aghassi-Hagmann, and Mehdi B Tahoori. An inkjet-printed low-voltage latch based on inorganic electrolyte-gated transistors. *IEEE Electron Device Letters*, 39(6):831–834, 2018.

[110] Wikipedia. ZILOG Z80. https://en.wikipedia.org/wiki/Zilog_Z80.

[111] wikipedia. ZILOGZPU. https://en.wikipedia.org/wiki/Zilog_Z80.

[112] A Willoughby. Design and processing of porous materials for electronic applications. *Philosophical transactions. Series A, Mathematical, physical, and engineering sciences*, 364:175–87, 02 2006.

[113] Wei Wu. Inorganic nanomaterials for printed electronics: a review. *Nanoscale*, 9(22):7342–7372, 2017.

[114] Wei Wu. Stretchable electronics: functional materials, fabrication strategies and applications. *Science and Technology of Advanced Materials*, 20(1):187–224, 2019.

[115] Yu Xia, Wei Zhang, Mingjing Ha, Jeong Ho Cho, Michael J Renn, Chris H Kim, and C Daniel Frisbie. Printed sub-2 v gel-electrolyte-gated polymer transistors and circuits. *Advanced Functional Materials*, 20(4):587–594, 2010.

[116] Wei Xiong, Yang Guo, Ute Zschieschang, Hagen Klauk, and Boris Murmann. A 3-v, 6-bit c-2c digital-to-analog converter using complementary organic thin-film transistors on glass. *IEEE Journal of Solid-State Circuits*, 45(7):1380–1388, 2010.

[117] D. C. Yacchirema, D. Sarabia-Jácome, C. E. Palau, and M. Esteve. A smart system for sleep monitoring by integrating iot with big data analytics. *IEEE Access*, 6:35988–36001, 2018.

[118] Bing Yin, Xiaomeng Liu, Hongyan Gao, Tianda Fu, and Jun Yao. Bioinspired and bristled microparticles for ultrasensitive pressure and strain sensors. *Nature communications*, 9(1):5161, 2018.

[119] Murat A Yokus, Cheyanne Hass, Talha Agcayazi, Alper Bozkurt, and Michael A Daniele. Towards a wearable perspiration sensor. In *2017 IEEE SENSORS*, pages 1–3. IEEE.

[120] Ki Jun Yu, Zheng Yan, Mengdi Han, and John A Rogers. Inorganic semiconducting materials for flexible and stretchable electronics. *NPJ Flexible Electronics*, 1(1):4, 2017.

[121] B. Zhai, S. Pant, L. Nazhandali, S. Hanson, J. Olson, A. Reeves, M. Minuth, R. Helfand, T. Austin, D. Sylvester, and D. Blaauw. Energy-efficient subthreshold processor design. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 17(8):1127–1137, Aug 2009.

[122] Wei Zhang. THE ORGANIC PROCESS DESIGN KIT (OPDK). http://opdk.umn.edu/index.html, 2014.

[123] Wei Zhang, Mingjing Ha, Daniele Braga, Michael J Renn, C Daniel Frisbie, and Chris H Kim. A 1v printed organic dram cell based on ion-gel gated transistors with a sub-10nw-per-cell refresh power. In *2011 IEEE International Solid-State Circuits Conference*, pages 326–328. IEEE, 2011.

[124] Jia Zhou, Tong Ge, and Joseph S Chang. Fully-additive printed electronics: Process development kit. In *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 862–865. IEEE, 2016.

[125] Chenxin Zhu, Alex Chortos, Yue Wang, Raphael Pfattner, Ting Lei, Allison Claire Hinckley, Igor Pochorovski, Xuzhou Yan, John W-F To, Jin Young Oh, et al. Stretchable temperature-sensing circuits with strain suppression based on carbon nanotube transistors. *Nature Electronics*, 1(3):183, 2018.

[126] Zinergy. Mk1-series ultrathin flexible printed batteries.

[127] Ute Zschieschang, Hagen Klauk, Marcus Halik, Günter Schmid, and Christine Dehm. Flexible organic circuits with printed gate electrodes. *Advanced materials*, 15(14):1147–1151, 2003.